ABSTRACT OF THE DISCLOSURE

A method for checking layout accuracy in an integrated circuit design includes creating a schematic, adding a line width marker to selected lines having a width greater than an absolute minimum width, and assigning a line width to each line width marker. A layout is created and is checked versus the schematic. A design is extracted from the layout. The design has a design line width corresponding to each line having a line width marker. The design line width is checked versus the marker line width for each line having a line width marker.